A SIMPLIFIED METHOD FOR LIMITING CLOCK PULSE WIDTH

ABSTRACT

The present invention provides for correcting excessive pulse widths using incremental delays. The pulse width is evaluated through a correction block and leak detector. An acceptable pulse passes through an interconnect directly to the clock output. Unacceptable pulses are sent through a block delay module that incorporates a series of delay sub-blocks that disconnect and reset in accordance with a pre-programmed total delay time. The conditioned clock pulse is resent through a node to the correction block and leak detector where it is reevaluated. If the pulse is acceptable, it is sent to the clock output. If the pulse is found unacceptable, it is recycled again. A high low clock pulse shuttle determines and alters the high or low state of the clock pulse to ensure a correct output to downstream dependent devices.